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Form PTO-1390	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER P20856
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/806479

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/03385	21 October 1999	21 October 1998

TITLE OF INVENTION

CIRCUIT ARRANGEMENT FOR ELECTRONICALLY GENERATING A RINGING IMPEDANCE

APPLICANT(S) FOR DO/EO/US

Jörg HAUPTMANN and Alexander KAHL

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. X This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ___ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. X This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. X The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. X A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. X is attached hereto (required only if not communicated by the International Bureau).
   b. ___ has been communicated by the International Bureau.
   c. ___ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. X An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)).
7. ___ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ___ are attached hereto (required only if not communicated by the International Bureau).
   b. ___ have been communicated by the International Bureau.
   c. ___ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ___ have not been made and will not be made.
8. ___ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3))
9. X An oath or declaration of the inventor(s) (35 U.S.C. .371(c)(4)). "Unexecuted"
10. X An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (U.S.C. 371(c)(5)).

Items 11 to 16 below concern other document(s) or information included:

11. Assignee: INFINEON TECHNOLOGIES AG of München, GERMANY
12. ___ An Information Disclosure Statement under 37 CFR 1.97 and 1.98
13. ___ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
14. X A FIRST preliminary amendment.
    ___ A SECOND or SUBSEQUENT preliminary amendment.
15. ___ A substitute specification.
16. ___ A change of power of attorney and/or address letter.
17. X Figure of Drawing to be published____1____
18. X Other items or information:
    Cover Sheet and International Application as published in German.
    PCT/IPEA/409-with five sheets of amended pages(in German).
    Five Sheets of amended pages.
    PCT/ISA/210(in English and German).
    Cover Letter under 35 USC 371 and 1.495.
    Claim of Priority.

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/806479	PCT/DE99/03385	P20856

19. ___ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)):		
Search report has been prepared by the EPO or JPO. . . . . $ 860.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482). . . . . $ 690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO(37 CFR 1.445(a)(2). . . . . $ 710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO. $1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4). . . . . $ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ___ 20 ___ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed		Number Extra	RATE		
Total Claims	20	- 20 =	0	X $18.00	$0.00	
Independent Claims	1	- 3 =	0	X $80.00	$0.00	
Multiple dependent claim(s) (if applicable)				+ $270.00	$0.00	
				TOTAL OF ABOVE CALCULATIONS =	$860.00	
___ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.					$	
				SUBTOTAL =	$860.00	
Processing fee of $130.00 for furnishing the English translation later than ___ 20 ___ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				+		
Extension of Time fee in the amount of $						
				TOTAL NATIONAL FEE =	$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property				+		
				TOTAL FEES ENCLOSED =	$860.00	
				Amount to be refunded		$
				Charged		$

a. X A check in the amount of $860.00 to cover the above fees is enclosed.

b. ___ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees.

c. X The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-0089.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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29,027
REGISTRATION NUMBER

P20856.A01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jörg HAUPTMANN et al.

Serial No. : Not Yet assigned (National Stage of PCT/DE99/03385)

Filed : Concurrently Herewith (International Filing Date October 21, 1999)

For : CIRCUIT ARRANGEMENT FOR ELECTRONICALLY GENERATING A RINGING IMPEDANCE

PRELIMINARY AMENDMENT

Commissioner of Patents and Trademarks
Washington, DC 20231

Sir :

Enclosed please find a copy of the International Preliminary Examination Report - Form PCT/IPEA/409 (hereinafter "Report") which was drawn on the originally filed description and drawings, and claims 1-13 as filed on October 21, 1999, and includes as an Annex amended page 1 of the specification and amended pages 16-19 including claims 1-13.

Based upon the submission of amended sheets of specification and claims, Applicants respectfully requests examination on the merits of the application containing amended pages 16-19 of claims 1-13, in place of originally filed claims 1-13 appearing on pages 16-19 of International Application No. PCT/DE99/03385 as originally filed.

Additionally, prior to the examination of the above-identified application including replacement claims 1-13, amendment of claims 1-13, as follows, and the addition of claims

14-20 are respectfully requested to remove multiple dependent claims, reference symbols, and to place the claims in accepted U.S. format.

IN THE CLAIMS

Please amend replacement claims 1-13, as follows (a marked-up copy of the claims is attached to this document):

1. (Amended-Clean Text) A circuit arrangement for electrically generating a ringing impedance in telephone terminals by means of at least one transistor and a capacitor, the ringing impedance being adaptable by controlling the resistance of the transistor, having a ringing alternating voltage which can be tapped between a first input terminal and a second input terminal, wherein a digital controller is provided for setting the ringing impedance, said controller adapting the ringing impedance to the given conditions by generating from the ringing alternating voltage a control voltage for controlling the transistor,

the digital controller has a programmable digital filter, and

the transmission function of the digital filter can be set by programing the associated filter coefficients.

2. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein the digital filter is a component of a programmable digital signal processor or microprocessor.

3. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein a digital power inverter circuit is connected upstream of the digital filter and a digital rectifier circuit is connected downstream of the digital filter.

4. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, comprising:

- a rectifier circuit for rectifying the ringing alternating voltage,
- a capacitor which is connected between an input terminal and rectifier circuit,
- a transistor which is arranged by means of its load path between the outputs of the rectifier circuit,
- a first and second voltage, which are rectified from the ringing alternating voltage by means of the rectifier circuit, being fed to the controller, and
- the controller making available a control voltage for driving the transistor.

5. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein the controller has an analog integrator circuit which is connected upstream of the transistor and which makes available an output signal which is integrated from the difference between a first input voltage and a second input voltage and which drives the transistor.

6. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein a voltage divider is provided which makes available a component voltage from the voltage which is present at the one output of the rectifier circuit.

7. (Amended-Clean Text) The circuit arrangement as claimed in claim 3, wherein the digital power inverter circuit , the digital filter and the digital rectifier circuit are together integrated on a semiconductor chip of digital design.

8. (Amended-Clean Text) The circuit arrangement as claimed in claim 3, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

9. (Amended-Clean Text) The circuit arrangement as claimed in claim 1, wherein

- a first capacitor, the load path of a first transistor and a first resistor are arranged in series between the first terminal and a reference potential,
- a second capacitor, the load path of a second transistor and a second resistor are arranged in series between the second terminal and the reference potential,
- a first and a second input potential of the ringing alternating voltage being fed to the controller and
- the controller making available a first control voltage for driving the first transistor and a second control voltage for driving the second transistor.

10. (Amended-Clean Text) The circuit arrangement as claimed in claim 9, wherein the controller

- has a first analog integrator circuit which is connected upstream of the first transistor and which makes available an output signal which is integrated from the difference between a first input voltage and a second input voltage and which drives the first transistor, and
- has a second analog integrator circuit which is connected upstream of the second transistor and which makes available an output signal which is integrated from the difference between a third input voltage and a fourth input voltage and which drives the second transistor.

11. (Amended-Clean Text) The circuit arrangement as claimed in claim 9, wherein a first voltage divider is provided which makes available a first component voltage from the first potential of the ringing alternating voltage, and

a second voltage divider is provided which makes available a second component voltage from the second potential of the ringing alternating voltage.

12. (Amended-Clean Text) The circuit arrangement as claimed in claim 10, wherein at least one analog/digital converter, which is connected upstream of the digital filter, is provided, and at least one digital/analog converter, which is connected downstream of the digital rectifier circuit, is provided, the analog/digital converters, the digital/analog

converters and the analog integrator circuits being together integrated on a semiconductor chip of analog design.

13. (Amended-Clean Text) The circuit arrangement as claimed claim 4, wherein at least one of the transistors is embodied as an n-channel-MOSFET.

Please add new claims 14-20 as follows:

---14. The circuit arrangement as claimed in claim 2, wherein a digital power inverter circuit is connected upstream of the digital filter and a digital rectifier circuit is connected downstream of the digital filter.

15. The circuit arrangement as claimed in claim 4, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

16. The circuit arrangement as claimed in claim 5, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

17. The circuit arrangement as claimed in claim 6, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

18. The circuit arrangement as claimed in claim 7, wherein an analog/digital converter is provided which is connected upstream of the digital power inverter circuit, and a digital/analog converter is provided which is connected downstream of the digital rectifier circuit, the analog/digital converter, the digital/analog converter and the analog integrator circuit being together integrated on a semiconductor chip of analog design.

19. The circuit arrangement as claimed in claim 2, wherein

- a first capacitor, the load path of a first transistor and a first resistor are arranged in series between the first terminal and a reference potential,
- a second capacitor, the load path of a second transistor and a second resistor are arranged in series between the second terminal and the reference potential,
- a first and a second input potential of the ringing alternating voltage being fed to the controller and
- the controller making available a first control voltage for driving the first transistor and a second control voltage for driving the second transistor.

20. The circuit arrangement as claimed in claim 10, wherein a first voltage divider is provided which makes available a first component voltage from the first potential of the ringing alternating voltage, and

a second voltage divider is provided which makes available a second component voltage from the second potential of the ringing alternating voltage.---

REMARKS

The Examiner is respectfully requested to enter the foregoing amendment prior to examination and calculation of the fees for the above-identified patent application.

The amendments to the claims made in this amendment have not been made to overcome the prior art, and thus, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Should there be any questions, the Examiner is invited to contact the undersigned at the below listed number.

Respectfully submitted,
Jörg HAUPTMANN et al.

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April 10, 2001
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MARKED-UP COPY OF THE CLAIMS

1. (Amended) A circuit arrangement for electrically generating a ringing impedance in telephone terminals by means of at least one transistor [(T1; T2, T3)] and a capacitor [(C; C1, C2)], the ringing impedance being adaptable by controlling the resistance of the transistor, having a ringing alternating voltage [(V~)] which can be tapped between a first input terminal [(a)] and a second input terminal, wherein [(b), characterized in that] a digital controller [(2, 4, 8; 2', 2", 4, 8', 8")] is provided for setting the ringing impedance, said controller adapting the ringing impedance to the given conditions by generating from the ringing alternating voltage [(V~)] a control voltage [(VSt)] for controlling the transistor [(T1)],

the digital controller [(2, 4, 8, 2', 2", 4, 8', 8")] has a programmable digital filter [(4)], and

the transmission function of the digital filter [(4)] can be set by programing the associated filter coefficients.

2. (Amended) The circuit arrangement as claimed in claim 1, wherein [characterized in that] the digital filter [(4)] is a component of a programmable digital signal processor [(4)] or microprocessor.

3. (Amended) The circuit arrangement as claimed in claim 1, wherein [one of claims 1 or 2, characterized in that] a digital power inverter circuit [(3)] is connected upstream of

the digital filter [(4)] and a digital rectifier circuit [(5)] is connected downstream of the digital filter.

4. (Amended) The circuit arrangement as claimed in claim 1, comprising: [one of the preceding claims, characterized by]

- a rectifier circuit [(1)] for rectifying the ringing alternating voltage [(V~)],
- a capacitor [(C)] which is connected between an input terminal [(a)] and rectifier circuit [(1)],
- a transistor [(T1)] which is arranged by means of its load path between the outputs [(12, 13)] of the rectifier circuit [(1)],
- a first and second voltage [(Va, Vb)], which are rectified from the ringing alternating voltage [(V~)] by means of the rectifier circuit [(12)], being fed to the controller [(2, 4, 8)], and
- the controller [(2, 4, 8)] making available a control voltage [(VSt)] for driving the transistor [(T1)].

5. (Amended) The circuit arrangement as claimed in claim 1, wherein [one of the preceding claims, characterized in that] the controller [(2, 4, 8)] has an analog integrator circuit [(8)] which is connected upstream of the transistor [(T1)] and which makes available an output signal [(VSt)] which is integrated from the difference between a first input voltage [(V1)] and a second input voltage [(Vb)] and which drives the transistor [(T1)].

6. (Amended) The circuit arrangement as claimed in claim 1, wherein [one of the preceding claims, characterized in that] a voltage divider [(R2, R3)] is provided which makes available a component voltage from the voltage [(Va)] which is present at the one output [(12)] of the rectifier circuit [(1)].

7. (Amended) The circuit arrangement as claimed in claim 3, [characterized in that] wherein the digital power inverter circuit [(3)], the digital filter [(4)] and the digital rectifier circuit [(5)] are together integrated on a semiconductor chip of digital design.

8. (Amended) The circuit arrangement as claimed in claim 3, wherein [one of claims 3 to 7, characterized in that] an analog/digital converter [(2)] is provided which is connected upstream of the digital power inverter circuit [(3)], and a digital/analog converter [(6)] is provided which is connected downstream of the digital rectifier circuit [(5)], the analog/digital converter [(2)], the digital/analog converter [(6)] and the analog integrator circuit [(8)] being together integrated on a semiconductor chip of analog design.

9. (Amended) The circuit arrangement as claimed in claim 1, wherein [or 2, characterized in that]

- a first capacitor [(C1)], the load path of a first transistor [(T2)] and a first resistor [(R10)] are arranged in series between the first terminal [(a)] and a reference potential [(VSS)],

- a second capacitor [(C2)], the load path of a second transistor [(T3)] and a second resistor [(R20)] are arranged in series between the second terminal [(b)] and the reference potential [(VSS)],

- a first and a second input potential [(Va~)] of the ringing alternating voltage [(V~)] being fed to the controller [(2', 2", 4, 8', 8")] and

- the controller [(2', 2", 4, 8', 8")] making available a first control voltage [(VSt1)] for driving the first transistor [(T2)] and a second control voltage [(VSt2)] for driving the second transistor [(T3)].

10. (Amended) The circuit arrangement as claimed in claim 9, [characterized in that] wherein the controller [(2', 2", 4, 8', 8")]

- has a first analog integrator circuit [(8')] which is connected upstream of the first transistor [(T2)] and which makes available an output signal [(VSt1)] which is integrated from the difference between a first input voltage [(VI1)] and a second input voltage [(Vam)] and which drives the first transistor [(T2)], and

- has a second analog integrator circuit [(8")] which is connected upstream of the second transistor [(T3)] and which makes available an output signal [(VSt2)] which is integrated from the difference between a third input voltage [(VI2)] and a fourth input voltage [(Vbm)] and which drives the second transistor [(T3)].

11. (Amended) The circuit arrangement as claimed in claim 9, wherein [or 10, characterized in that] a first voltage divider [(R30, R50)] is provided which makes available a first component voltage from the first potential [(Va~)] of the ringing alternating voltage [(V~)], and

a second voltage divider [(R40, R60)] is provided which makes available a second component voltage from the second potential [(Vb~)] of the ringing alternating voltage [(V~)].

12. (Amended) The circuit arrangement as claimed in claim 10, wherein [or 11, characterized in that] at least one analog/digital converter [(2', 2")], which is connected upstream of the digital filter [(4)], is provided, and at least one digital/analog converter [(6', 6")], which is connected downstream of the digital rectifier circuit [(5)], is provided, the analog/digital converters [(2', 2")], the digital/analog converters [(6', 6")] and the analog integrator circuits [(8', 8")] being together integrated on a semiconductor chip of analog design.

13. (Amended) The circuit arrangement as claimed claim 4, wherein [in one of claims 4 to 12, characterized in that] at least one of the transistors [(T1; T2, T3)] is embodied as an n-channel-MOSFET.

Description

Circuit arrangement for electronically generating a ringing impedance

The present invention relates to a circuit arrangement as claimed in the preamble of patent claim 1, as is known from US 5,485,516.

In analog telecommunications systems, in order to notify a subscriber of an incoming call, a ringing signal is transmitted to the terminal of the subscriber. This ringing signal takes the form of a sinusoidal alternating voltage, the so-called ringing voltage or ringing alternating voltage. The called subscriber terminal has to detect the ringing signal and when necessary react to the ringing signal (for example by notifying the called subscriber by means of a ringing tone or by connecting to the line). In order to adapt to the telephone line, subscriber terminals form ringing impedances which have to satisfy different requirements owing to the differing design of the telephone networks in different countries. In Germany, the ringing impedance requirements can be obtained from the requirement catalog of the Bundespost [German Federal postal service] BAPT 223 ZV5, issue 5.2.1994, page 12; chapter 2.6.1 Ringing Impedance.

In telephone terminals, ringing impedances are usually formed from a resistor and a capacitor, the resistor forming the resistive part, and the capacitor the capacitive part, of a ringing impedance. The values of the resistor and capacitor must be adapted here to the requirements for a particular country, which requirements prescribe specific values for the ringing impedance. Owing to these requirements, a telephone terminal must have a specific design for a particular country. The disadvantage here is

country. The disadvantage here is the increased expenditure on the production of subscriber terminals because a separate subscriber terminal variant which fulfils the ringing impedance requirements has to be manufactured for each country.

From US 5,485,516 it is known to make the line impedance of a telephone line adaptable to the line conditions, for example the transmission characteristics, by means of a transistor and a controller which controls this transistor. However, the ringing impedance is implemented here with a capacitor and a resistor, and both have to be adapted in a specific way for a particular country.

The invention is therefore based on the technical object of making available a circuit arrangement of the type mentioned at the beginning in which the ringing impedance can be adapted easily, and yet as flexibly as possible, to the given conditions by circuit means.

This objective is achieved according to the invention by means of a circuit arrangement having the features of patent claim 1.

Accordingly, a circuit arrangement of the type mentioned at the beginning is made available in which a controller is provided for setting the impedance, said controller adapting the ringing impedance to the given conditions and having a programmable digital filter, and it being possible to set the transmission function of the controller by programming the filter coefficients of the digital filter.

Advantageous refinements of the circuit arrangement emerge from the respective subclaims.

The controller according to the invention can be used to program the ringing impedance and thus adapt it to the respectively desired conditions, for example to a very wide range of different specific requirements for particular countries. For this purpose, the controller has a digital filter which can be programmed, for example, by means of a program-

controlled unit. The transmission function of the controller, and thus the ringing impedance, can be set by programming the filter coefficients of the digital filter. In one advantageous embodiment, the program-controlled unit is embodied as a known microprocessor, for example a digital signal processor (DSP). In a particularly preferred embodiment, the digital filter is implemented in the form of a program in the digital signal processor.

This provides advantages in particular when producing subscriber terminals, because the design of a subscriber terminal is uniform and the country in which the subscriber terminal can be used is determined only by setting the transmission function of the controller.

In one preferred embodiment, the circuit arrangement forms the ringing impedance by means of a capacitor, which is connected between a first terminal for a two-wire line and a rectifier, and a transistor whose load path is connected between a first output of the rectifier and a reference potential. The transistor is controlled by a controller, the transmission function of the controller being adjustable in order to adapt the ringing impedance to specific requirements for particular countries. In particular, advantages are obtained when producing subscriber terminals because the design of a subscriber terminal is uniform and the country in which the subscriber terminal can be used is determined only by setting the transmission function of the controller.

In one preferred embodiment, a digital power inverter circuit is connected upstream of the digital filter. In a further preferred embodiment, a digital rectifier circuit is connected downstream of the digital filter.

In one preferred embodiment, the controller has an analog integrator circuit which is connected upstream of the transistor and which integrates the difference between a first input voltage and a second

input voltage and whose output signal controls the transistor.

In a further preferred embodiment, a voltage divider divides the voltage present at the first output of the rectifier into a smaller voltage.

In a particularly preferred embodiment, the digital power inverter circuit, the digital filter and the digital rectifier circuit are integrated on one digital module.

In a preferred embodiment, the analog/digital converter, the digital/analog converter and the analog integrator circuit are integrated on one analog module.

In a further preferred embodiment, the controller has a first analog integrator circuit which is connected upstream of the control terminal of the first transistor and which integrates the difference between a first input voltage and a second input voltage and whose output signal controls the first transistor, and a second analog integrator circuit which is connected upstream of the control terminal of the second transistor and which integrates the difference between a third input voltage and a fourth input voltage and whose output signal controls the second transistor. This circuit arrangement advantageously has no need of a rectifier circuit for rectifying the ringing alternating voltage.

A first voltage divider preferably divides the first potential of the ringing alternating voltage, and a second voltage divider preferably divides the second potential of the ringing alternating voltage.

In one preferred embodiment, a first and a second analog/digital converter, a first and a second digital/analog converter and the first and second analog integrator circuits are integrated on one analog module.

In a preferred embodiment, the transistors are embodied as n-channel MOSFETs.

Further advantageous embodiments and developments of the invention can be found in the subclaims, the following description and the figures.

The invention is explained in more detail below by means of an advantageous exemplary embodiment which is given in the figures of the drawing, in which:

Fig. 1 shows a first exemplary embodiment of a circuit arrangement for electronically generating a ringing impedance;

Fig. 2 shows a timing diagram with a digital input signal and the digital output signal, calculated therefrom, of a digital power inverter circuit;

Fig. 3 shows a voltage-controlled power source for setting the conduction current according to figure 1;

Fig. 4 shows a second exemplary embodiment of a circuit arrangement for electronically generating a ringing impedance;

Fig. 5 shows two voltage-controlled power sources for setting a first and second conduction current according to figure 4.

In all the figures of the drawing, identical or functionally identical elements and signals are provided with identical reference symbols.

The circuit arrangement illustrated in fig. 1 for electronically generating a ringing impedance has two terminals a and b which can be connected to a two-wire line of a telephone network. Ringing signals can be received from another subscriber via the two-wire line, the ringing signals being generated by means of a sinusoidal alternating voltage V~ with the frequency fR. This alternating voltage becomes the ringing alternating voltage below. The switch S, which corresponds to the hook switch, is open with the result that direct signal elements in the ringing signal are blocked by means of a capacitor C.

The capacitor C simultaneously forms a capacitive part of the ringing impedance. Connected

downstream of the capacitor C is a bridge rectifier 1 which rectifies the ringing alternating voltage. The following circuits are provided with voltage from the rectified ringing alternating voltage. Furthermore, the rectified ringing alternating voltage ensures the setting of the conduction current I which is used to set the ringing impedance. A rectified positive ringing alternating voltage Va or negative ringing alternating voltage Vb is applied to a first output 12 and a second output 13 of the bridge rectifier 1, respectively. The rectified positive ringing alternating voltage Va and negative ringing alternating voltage Vb are referred to a reference potential VSS, the amplitude of the rectified positive ringing alternating voltage Va being much greater than the amplitude of the rectified negative ringing alternating voltage Vb.

The first output 12 and second output 13 of the bridge rectifier 1 are connected to the reference potential VSS via a transistor T1 and a resistor R1, respectively. The transistor T1 forms, in combination with the capacitor C, the ringing impedance. The ringing impedance can be adapted to the various requirements which are specific to particular countries by controlling the resistance of the transistor T1. For this purpose, a control voltage VSt for the transistor T1 is derived from the rectified positive ringing alternating voltage Va and negative ringing alternating voltage Vb using a digital controller.

The rectified positive ringing alternating voltage Va, which has high voltage values, is divided into a smaller voltage by means of a voltage divider R2 and R3, in order to be processed by the following circuits in which signals have only low voltage levels in comparison with the rectified positive ringing alternating voltage.

The voltage-divided positive ringing alternating voltage Va and the negative ringing alternating voltage Vb are fed to a subtractor circuit 7 at whose output a difference voltage Vab is present.

The difference voltage Vab is subsequently sampled by a first analog/digital converter 2 with a sampling rate fs and converted into a digital signal V'ab.

The digital signal V'ab is fed to a first digital power inverter circuit 3. Figure 2 illustrates a timing diagram with the digital input and output signals of the digital power inverter circuit. If the digital values V'ab drop below a lower predefinable threshold value MIN at the input of the first digital power inverter circuit 3, a counter begins to count with the sampling rate fs/N of the digital signal. If the counter reading exceeds a predefinable value which can be set by a digital control device 10 in accordance with the frequency of the ringing alternating voltage, the digital values at the output V'ab~ of the first digital power inverter circuit 3 are inverted by reversing their sign after a waiting time TS expires. During the waiting time TS, the counter remains reset and does not begin to count again until the digital values V'ab drop below the threshold value MIN at the input. A digital output signal, which constitutes a first ringing alternating voltage referred to the reference potential VSS, is thus generated from the digital input signal which constitutes a rectified sinusoidal oscillation - the ringing alternating voltage referred to the reference potential VSS.

The digital output signal of the digital power inverter circuit 3 is fed to a digital filter 4. For adaptation to specific requirements for particular countries, the digital filter 4 can be programmed by means of a digital control device 10 in order to be able to adapt the ringing impedance, and for this purpose it has a programmable transmission function k. For this purpose, the phase shift and amplification which are necessary for the ringing impedance are calculated from the input signal V'ab~ by means of the digital filter 4. The digital filter 4 can be embodied here as a digital hardware filter in which the

coefficients are programmable. The digital filter can likewise be embodied as a signal processing algorithm on a digital signal processor, the filter function being adjustable for various ringing impedances by means of variables.

A digital rectifier circuit 5 rectifies the digital output signal of the digital filter 4 VSI~ by forming absolute values.

The output signal VSI of the digital rectifier circuit 5 is converted into an analog signal VI by a digital/analog converter 6.

The analog signal VI is fed to a first input of an analog integrator circuit 8. The negative ringing alternating voltage Vb, which is proportional to the conduction current, is fed to the analog integrator circuit 8 via a second input. A difference, which is subsequently integrated, is formed in the analog integrator circuit 8 from the two input signals. The output signal VSt of the analog integrator circuit 8 is fed to the control terminal of the transistor T1. The transistor T1 is set by means of the supplied voltage VSt.

Figure 3 illustrates the adjustability of the conduction current I by means of the transistor T1. The analog signal VI of the digital controller and the negative ringing alternating voltage Vb, which is proportional to the conduction current, are fed to a subtractor circuit 21 at whose output the difference voltage VI - Vb is present. The difference voltage VI - Vb is integrated by an integrator circuit. The voltage VSt which is fed to the control terminal of the transistor T1 is present at the output of the integrator circuit 20. The conduction current I is set by means of the transistor T1. The integrator circuit 20 integrates the difference voltage VI - Vb until the difference voltage VI - Vb = 0. A conductance value GM = I/VI = 1/R1 can be derived from this using Vb = R1*I = VI.

The conduction current I is thus controlled by means of the analog signal VI of the digital controller in such a way that the necessary ringing impedance Z is calculated for a difference voltage Vab from the amplification factor ksense of the voltage divider R2 and R3, the transmission function k of the digital filter 4 and the conductance value GM of the analog integrator circuit:

$$Z = \frac{Vab}{I} = \frac{1}{ksense \cdot k \cdot GM} = \frac{R1}{ksense} = f(k)$$

The conduction current I can thus be set by means of the transistor T1. The transistor T1 can in turn be set by means of the programmable transmission function k of the digital filter 4. The ringing impedance thus depends on the programmable transmission function k of the digital filter 4 and can be adapted to various specific requirements for particular countries by simply reprogramming the transmission function k of the digital filter 4. To do this, specific values for a particular country can be stored for the ringing impedance in a memory 11, for example. The digital control device 10 reads out of the memory 11 the values from the memory 11 which are necessary for programming a specific ringing impedance for a particular country, programs the digital filter 4 accordingly and sets the digital power inverter 3 to the frequency fR of the ringing alternating voltage.

The circuit arrangement illustrated in fig. 4 for electronically generating a ringing impedance has a first terminal a and a second terminal b which can be connected to a two-conductor subscriber line. Ringing signals can be received via the two-wire line, the ringing signals being generated by a sinusoidal alternating voltage V~ with a frequency fR. Direct signal elements in the ringing signal are blocked by means of a first capacitor C1 and a second capacitor C2.

The first capacitor C1 and the second capacitor C2 also form a capacitive part of a ringing impedance.

A first series circuit composed of the first capacitor C1, the load path of a first transistor T2 and a first resistor R10 is provided for the positive half-wave of the ringing alternating voltage V~. The series circuit connects the first terminal a to a reference potential VSS. A first potential Va~ of the ringing alternating voltage V~ can be tapped at the connecting point of the first capacitor C1 and of the first transistor T2.

A second series circuit composed of the second capacitor C2, the load path of a second transistor T3 and a second resistor R20 is provided for the negative half-wave of the ringing alternating voltage V~. The series circuit connects the second terminal b to the reference potential VSS. A second potential Vb~ of the ringing alternating voltage Vb~ can be tapped at the connecting point of the second capacitor C2 and of the second transistor T3.

The ringing impedance is formed in each case for the positive or negative half-wave of the ringing alternating voltage V~ by the first capacitor C1 and the first transistor T2 or the second capacitor C2 and the second transistor T3. To do this, a first conduction current I1 and a second conduction current I2 are respectively set in the first and second series circuits respectively.

For the positive half-wave, the second transistor T3 is connected with low impedance so that the second series circuit between the second terminal b and the reference potential VSS has low impedance. For the negative half-wave, the first transistor T2 is connected with low impedance, so that the first series circuit between the first terminal a and the reference potential VSS has low impedance.

The first potential Va~ (positive half-wave) is divided by a first voltage divider R30 and R50 into a

smaller voltage which is converted into a first digital signal V'a~ by a first analog/digital converter 2'.

The second potential Vb~ (negative half-wave) is divided by a second voltage divider R40 and R60 into a smaller voltage which is converted into a second digital signal V'b~ by a second analog/digital converter 2'.

The first digital signal V'a~ and the second digital signal V'b~ are fed to a digital filter 4 (impedance filter).

The digital filter 4 is programmed by a control unit 10 - for example a microprocessor - which is connected to a memory 11. The programming of the digital filter 4 serves here to set specific parameters of the ringing impedance for particular countries. To do this, different specific data for particular countries can be stored in the memory 11. Depending on the area of application of the circuit arrangement, the control unit 10 reads the specific data for a particular country out of the memory 11 and correspondingly programs the digital filter 4.

The digital filter 4 generates a first digital output signal VSI1 and a second digital output signal VSI2.

The first digital output signal VSI1 is converted by a first digital/analog converter 6' into a first input signal VI1 for a first analog integrator circuit 8'.

In parallel, the second digital output signal VSI2 is converted by a second digital/analog converter 6'' into a second input signal VI2 for a second analog integrator circuit 8''.

The first analog integrator circuit 8' integrates the difference between the first input signal VI1 and a second input signal Vam which is tapped at the connecting point of the load path of the first transistor T2 and of the first resistor R10. The second input signal Vam = R10*I1 depends here on the first conduction current I1.

In parallel, the second analog integrator circuit 8'' integrates the difference between the first input signal VI2 and a second input signal Vbm which is tapped at the connecting point of the load path of the second transistor T3 and of the second resistor R20. The second input signal Vbm = R20*I2 depends here on the second conduction current I2.

Figure 5 illustrates the design of the first and second analog integrator circuits and the adjustability of the first conduction current I1 and of the second conduction current I2 by means of the first transistor T2 or the second transistor T3.

The first analog control signal VI1 and the potential Vam, which is tapped at the connecting point of the load path of the first transistor T2 and of the first resistor R10, are fed to a first subtractor circuit 12 at whose output a difference voltage VI1 - Vam is present. The difference voltage VI1 - Vam is integrated by a first integrator circuit 11. A voltage VSt1 which is fed to the control terminal of the first transistor T2 is present at the output of the first integrator circuit 11. The first conduction current I1 is set by means of the first transistor T2. The first integrator circuit 11 integrates the difference voltage VI1 - Vam until the difference voltage VI1 - Vam = 0. A conductance value GM1 = I1/VI1 = 1/R10 can be derived from this using Vam = R10*I1 = VI1.

The first conduction current I1 is thus controlled by means of the first analog signal VI1 of the digital controller in such a way that the necessary ringing impedance Z1, given a positive half-wave of the ringing alternating voltage V~, is calculated from the amplification factor ksense1 of the first voltage divider R30 and R50, a first transmission function k1 of the digital filter 4 and the conductance value GM1 of the first analog integrator circuit 8':

$$Z1 = \frac{Va\ \sim}{I1} = \frac{1}{ksense1 \cdot k1 \cdot GM1} = \frac{R10}{ksense1 \cdot k1} = f_1(k1)$$

The first conduction current I1 can thus be set by means of the first transistor T2. The first transistor T2 can in turn be set by means of the programmable first transmission function k1 of the digital filter 4. The ringing impedance thus depends on the programmable first transmission function k1 of the digital filter 4 and can be adapted to various specific requirements for particular countries by simply reprogramming the first transmission function k1 of the digital filter 4. To do this, specific values for the ringing impedance for particular countries can be stored in the memory 11, for example. The control device 10 reads out of the memory 11 the values which are necessary for programming a specific ringing impedance for a particular country and reprograms the first transmission function k1 of the digital filter 4 accordingly.

The second analog control signal VI2 and the potential Vbm which is tapped at the connecting point of the load path of the second transistor T3 and of the second resistor R20 are fed to a second subtractor circuit 22 at whose output a difference voltage VI2 - Vbm is present. The difference voltage VI2 - Vbm is integrated by a second integrator circuit 21. A voltage VSt2 which is fed to the control terminal of the second transistor T3 is present at the output of the second integrator circuit 21. The second conduction current I2 is set by means of the second transistor T3. The second integrator circuit 21 integrates the difference voltage VI2 - Vbm until the difference voltage VI2 - Vbm = 0. A conductance value GM2 = I2/VI2 = 1/R20 can be derived from this using Vbm = R20*I2 = VI2.

The second conduction current I2 is thus controlled by means of the second analog signal VI2 of the digital controller in such a way that the necessary ringing impedance Z2, given a negative half-wave of the ringing alternating voltage V~, is calculated from the amplification factor ksense2 of the second voltage

divider R40 and R60, a second transmission function k2 of the digital filter 4 and the conductance value GM2 of the second analog integrator circuit 8'' as:

$$Z2 = \frac{Vb\sim}{I2} = \frac{1}{ksense2 \cdot k2 \cdot GM2} = \frac{R20}{ksense2 \cdot k2} = f_2(k2)$$

The second conduction current I2 can thus be set by means of the second transistor T3. The second transistor T3 can be set in turn by means of the programmable second transmission function k2 of the digital filter 4. The ringing impedance thus depends on the programmable second transmission function k2 of the digital filter 4 and can be adapted to various specific requirements for particular countries by simply reprogramming the second transmission function k2 of the digital filter 4. The reprogramming of the second transmission function k2 is carried out here in a way analogous to the reprogramming of the first transmission function k1.

The first transmission function k1 and the second transmission function k2 are preferably identical, so that the same ringing impedance Z_{total} is respectively set for either a positive or negative half-wave of the ringing alternating voltage V~. This presumes, of course, identical conductance values GM1 and GM2 of the first analog integrator circuit 8' and second analog integrator circuit 8'' and identical voltage divider ratios of the first and second voltage dividers. Thus, with GM1 = GM2 and ksense1 = ksense2, the ringing impedance Z_{total} obtained is:

$$Z_{total} = Z1 = Z2.$$

However, with the circuit arrangement according to the invention, it is also possible to set an asymmetrical ringing impedance which has a different ringing impedance Z1 for the positive half-wave of the ringing

alternating voltage V~ than for the negative half-wave of the ringing alternating voltage V~.

Patent claims

1. A circuit arrangement for electrically generating a ringing impedance in telephone terminals by means of at least one transistor (T1; T2, T3) and a capacitor (C; C1, C2), the ringing impedance being adaptable by controlling the resistance of the transistor, having a ringing alternating voltage (V~) which can be tapped between a first input terminal (a) and a second input terminal (b), characterized in that a digital controller (2, 4, 8; 2', 2'', 4, 8', 8'') is provided for setting the ringing impedance, said controller adapting the ringing impedance to the given conditions by generating from the ringing alternating voltage (V~) a control voltage (VSt) for controlling the transistor (T1),
the digital controller (2, 4, 8, 2', 2'', 4, 8', 8'') has a programmable digital filter (4), and
the transmission function of the digital filter (4) can be set by programming the associated filter coefficients.

2. The circuit arrangement as claimed in claim 1, characterized in that the digital filter (4) is a component of a programmable digital signal processor (4) or microprocessor.

3. The circuit arrangement as claimed in one of claims 1 or 2, characterized in that a digital power inverter circuit (3) is connected upstream of the digital filter (4) and a digital rectifier circuit (5) is connected downstream of the digital filter.

4. The circuit arrangement as claimed in one of the preceding claims, characterized by

- a rectifier circuit (1) for rectifying the ringing alternating voltage (V~),
- a capacitor (C) which is connected between an input terminal (a) and rectifier circuit (1),

- a transistor (T1) which is arranged by means of its load path between the outputs (12, 13) of the rectifier circuit (1),
- a first and second voltage (Va, Vb), which are rectified from the ringing alternating voltage (V~) by means of the rectifier circuit (12), being fed to the controller (2, 4, 8), and
- the controller (2, 4, 8) making available a control voltage (VSt) for driving the transistor (T1).

5. The circuit arrangement as claimed in one of the preceding claims, characterized in that the controller (2, 4, 8) has an analog integrator circuit (8) which is connected upstream of the transistor (T1) and which makes available an output signal (VSt) which is integrated from the difference between a first input voltage (VI) and a second input voltage (Vb) and which drives the transistor (T1).

6. The circuit arrangement as claimed in one of the preceding claims, characterized in that a voltage divider (R2, R3) is provided which makes available a component voltage from the voltage (Va) which is present at the one output (12) of the rectifier circuit (1).

7. The circuit arrangement as claimed in claim 3, characterized in that the digital power inverter circuit (3), the digital filter (4) and the digital rectifier circuit (5) are together integrated on a semiconductor chip of digital design.

8. The circuit arrangement as claimed in one of claims 3 to 7, characterized in that an analog/digital converter (2) is provided which is connected upstream of the digital power inverter circuit (3), and a digital/analog converter (6) is provided which is connected downstream of the digital rectifier circuit (5), the analog/digital converter (2), the digital/analog converter (6) and the analog integrator

circuit (8) being together integrated on a semiconductor chip of analog design.

9. The circuit arrangement as claimed in claim 1 or 2, characterized in that

- a first capacitor (C1), the load path of a first transistor (T2) and a first resistor (R10) are arranged in series between the first terminal (a) and a reference potential (VSS),
- a second capacitor (C2), the load path of a second transistor (T3) and a second resistor (R20) are arranged in series between the second terminal (b) and the reference potential (VSS),
- a first and a second input potential (Va~) of the ringing alternating voltage (V~) being fed to the controller (2', 2'', 4, 8', 8''), and
- the controller (2', 2'', 4, 8', 8'') making available a first control voltage (VSt1) for driving the first transistor (T2) and a second control voltage (VSt2) for driving the second transistor (T3).

10. The circuit arrangement as claimed in claim 9, characterized in that the controller (2', 2'', 4, 8', 8'')

- has a first analog integrator circuit (8') which is connected upstream of the first transistor (T2) and which makes available an output signal (VSt1) which is integrated from the difference between a first input voltage (VI1) and a second input voltage (Vam) and which drives the first transistor (T2), and
- has a second analog integrator circuit (8'') which is connected upstream of the second transistor (T3) and which makes available an output signal (VSt2) which is integrated from the difference between a third input voltage (VI2) and a fourth input voltage (Vbm) and which drives the second transistor (T3).

11. The circuit arrangement as claimed in claim 9 or 10, characterized in that a first voltage divider (R30, R50) is provided which makes available a first component voltage from the first potential (Va~) of the ringing alternating voltage (V~), and
a second voltage divider (R40, R60) is provided which makes available a second component voltage from the second potential (Vb~) of the ringing alternating voltage (V~).

12. The circuit arrangement as claimed in claim 10 or 11, characterized in that at least one analog/digital converter (2', 2''), which is connected upstream of the digital filter (4), is provided, and at least one digital/analog converter (6', 6''), which is connected downstream of the digital rectifier circuit (5), is provided, the analog/digital converters (2', 2''), the digital/analog converters (6', 6'') and the analog integrator circuits (8', 8'') being together integrated on a semiconductor chip of analog design.

13. The circuit arrangement as claimed in one of claims 4 to 12, characterized in that at least one of the transistors (T1; T2, T3) is embodied as an n-channel-MOSFET.

Memory
Impedance filter
10
11
4
3
5
2
6
7
8
GM
R1
R2
R3
T1
VSS
Vab~
V'ab
VSI~
VSI
VI
Vab
Va
Vb
V~
S
C
a
b
12
13

FIG 1

FIG 2

Predefined counter reading
Counting pulses
TS
MIN
Is/N
Vab
Vab
t

FIG 3

I
T1
VSS
R1
VSt
Vb
20
21
GM
VI

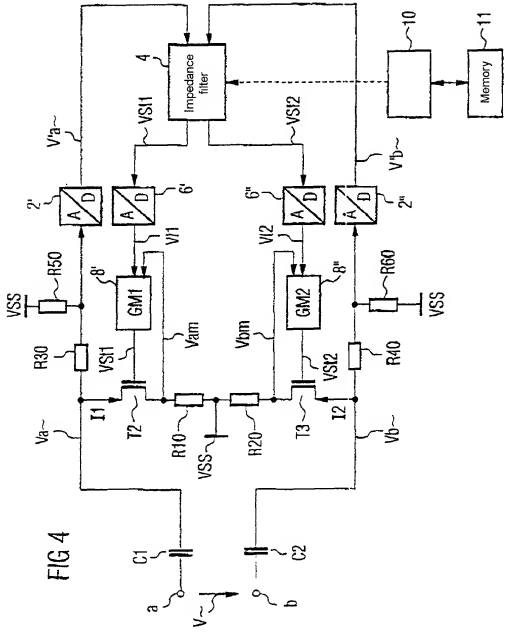
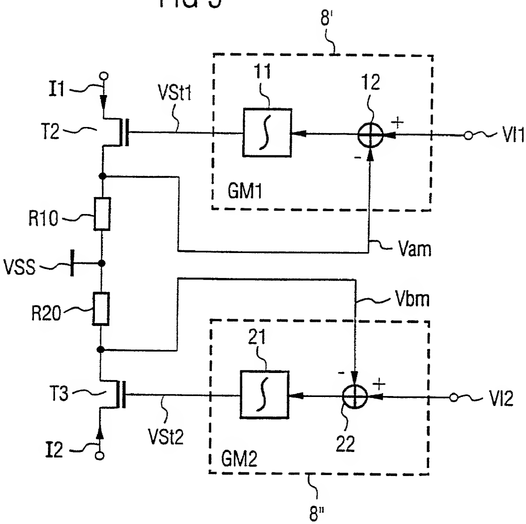

Impedance filter
4
10
11
Memory
VSI1
VSI2
Va
Vb
2'
2"
6'
6"
A/D
VI1
VI2
8'
8"
GM1
GM2
R50
R60
VSS
R30
R40
VSI1
VSI2
Vam
Vbm
I1
I2
T1
T2
T3
R10
R20
Va
Vb
C1
C2
a
b
V

FIG 4

FIG 5



Declaration and Power of Attorney For Utility or Design Patent Application

Erklärung für Patentanmeldungen zur Gebrauchseignung und Entwicklung
mit Vollmacht

S0757

German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

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My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CIRCUIT ARRANGEMENT FOR ELECTRONICALLY GENERATING A RINGING IMPEDANCE

deren Beschreibung hier beigefügt ist, es sei denn (in diesem Falle Zutreffendes bitte ankreuzen), diese Erfindung

the specification of which is attached hereto unless the following box is checked:

☒ wurde angemeldet am 21 October 1999
unter der US-Anmeldenummer 09/806,479
und wurde am Apr.11,2001 abgeändert (falls zutreffend)
oder

☒ was filed on October 21, 1999 as United States Application Number 09/806,479 and was amended on Apr.11, 2001 (if applicable)
or,

☐ unter der PCT internationalen Anmeldungsnummer PCT/DE99/03385 und wurde am _____ abgeändert (falls zutreffend).

☐ PCT International Application Number PCT/DE99/03385 and was amended on _____ (if applicable).

Ich bestätige hiermit, daß ich den Inhalt der oben angegebene Patentanmeldung einschließlich der Ansprüche, die eventuell durch einen oben erwähnten Zusatzantrag abgeändert wurde, durchgesehen und verstanden habe.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Titel 37, Code of Federal Regulations, § 1.56 von Belang sind.

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Prior Foreign Applications
Frühere ausländische Anmeldungen

			Priority Claimed Prioritätsanspruch	
198 48 606.5	GERMANY	21/OCTOBER/1998	☒	☐
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Nummer)	(Land)	(Tag/Monat/Jahr der Anmeldung)	Ja	Nein
198 58 761.9	GERMANY	18/DECEMBER/1998	☒	☐
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Nummer)	(Land)	(Tag/Monat/Jahr der Anmeldung)	Ja	Nein

☐ Zusätzliche einstweilige Anmeldungsnummern sind im Prioritätsanhang aufgeführt.

☐ Additional foreign application numbers are listed on a supplemental priority sheet attached hereto.

German La[illegible]age Utility or Design Patent Applic[illegible]n Declaration

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I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

(Application Number) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)
(Application Number) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)
(Application Number) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)

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☐ Additional provisional application numbers are listed on a supplemental priority sheet attached hereto.

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I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application No.) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	(Status) (patentiert, schwebend, aufgegeben) (patented, pending, abandoned)
(Application No.) (Aktenzeichen)	(Day/Month/Year Filed) (Tag/Monat/Jahr eingereicht)	(Status) (patentiert, schwebend, aufgegeben) (patented, pending, abandoned)

☐ Zusätzliche USA oder internationale Anmeldungsnummern sind im ergänzenden Prioritätsanhang aufgeführt.

☐ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

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KUNDENNUMMER 7055

CUSTOMER NUMBER 7055

Die ernannten Patenanwälte sind zur Zeit:

The appointed attorneys presently include:

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Bruce H. Bernstein	Reg. No. 29,027	Leslie J. Paperner	Reg. No. 33,329
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Unterschrift des Erfinders Datum 8.06.01	Inventor's signature Date 8.06.01
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Vor-und Nachname des zweiten Miterfinders (falls zutreffend) Alexander KAHL	Full name of second joint inventor, if any Alexander KAHL
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(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).	(Supply similar information and signature for third and subsequent joint inventors).